IN THE CLAIMS:

Please amend the claims as follows (all claims listed):

Claims 1.-20. (Cancelled)

21. (Currently Amended) A method of pausing processing of instructions, comprising:

determining whether a first instruction for a first thread is an instruction of a first type at a pipeline stage of a processor;

pausing processing of instructions of said first thread at said pipeline stage for a period of time if said first instruction is of a first type while processing instructions from a second thread at said pipeline stage; and

resuming processing of instructions of said first thread ~~responsive~~ in response to the determining operation at said pipeline stage.

22. (Previously Presented) The method of claim 21 further comprising decoding said first instruction into a first microinstruction and a second microinstruction.

23. (Previously Presented) The method of claim 22 wherein said first microinstruction causes a value to be stored in memory for said first thread.

24. (Previously Presented) The method of claim 23 further comprising:

processing said second microinstruction for execution when said value stored in memory is reset.

25. (Previously Presented) The method of claim 24 wherein said value stored in memory is reset if said first microinstruction is retired.

26. (Currently Amended) A method comprising:

determining at a pipeline stage whether a first instruction of a first thread is an instruction of a first type;

initiating a counter if said first instruction is an instruction of the first type; and

pausing processing of instructions of said first thread at ~~a~~ the pipeline stage of a processor until said counter reaches a predetermined value while processing instructions for a second thread at said pipeline stage.

27. (Previously Presented) The method of claim 26 wherein said first instruction includes an operand and said initiating includes loading said counter with said operand.

28. (Previously Presented) The method of claim 27 further comprising resuming processing instructions of said first thread after said counter reaches said predetermined value.

29. (Currently Amended) An apparatus, comprising:

a decode unit to determine whether a first instruction of a first thread is an instruction of a first type, said decode unit to pause processing of instructions of said first thread at a pipeline stage of a processor for a period of time if said first instruction is an instruction of the first type while instructions from a second thread can be processed, said decode unit further to cause resumption of processing instructions of said first thread in response to the determination at said decode unit.

30. (Previously Presented) The apparatus of claim 29 wherein said first instruction comprises a first microinstruction and a second microinstruction.

31. (Previously Presented) The apparatus of claim 30 further comprising:

a memory, wherein the determination at said decode unit is to cause a value to be stored in memory for said first thread.

32. (Previously Presented) The apparatus of claim 31 wherein said decode unit is to process said second microinstruction if said value stored in memory is reset.

33. (Previously Presented) The apparatus of claim 32 further comprising:

a retire unit coupled to said decode unit wherein said retire unit is to cause said value stored in memory to be reset if said first microinstruction is retired by said retire unit.

34. (Previously Presented) An apparatus comprising:

a decode unit to determine whether a first instruction for a first thread is an instruction of a first type;

a counter coupled to said decode unit, said counter to be initiated if said first instruction for said first thread is an instruction of said first type, said decode unit to pause processing instructions of said first thread at a pipeline stage of a processor until said counter reaches a predetermined value; and

wherein instructions for a second thread can be processed while instructions of said first thread are paused from being processed and wherein said decode unit is to resume processing instructions of said first thread in response to the determination at said decode unit.

35. (Previously Presented) The apparatus of claim 34 wherein said first instruction includes an operand to be loaded into said counter.

36. (Previously Presented) The apparatus of claim 35 wherein said decode unit can continue to operate while said first thread is paused from being processed.